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**LINEARITY AND EFFICIENCY
PERFORMANCE OF GaN HEMTs
WITH DIGITAL PRE-DISTORTION
CORRECTION (PREPRINT)**



**M.J. Poulton, W.K. Leverich, J.B. Shealy, R. Vetur, J. Brown,
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Linearity and Efficiency Performance of GaN HEMTs with Digital Pre-Distortion Correction

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Abstract — The linearity and efficiency performance was studied for large periphery AlGaN/GaN HEMTs. Comparison was made between inherent linear device performance and device performance using Digital Pre-Distortion (DPD) correction. Additionally, both drain voltage and current were optimized to provide high efficiency for a specified linearity. Significant improvements in linear efficiency were achieved using the DPD correction with a best measured PAE of 43.5 %, at a V_d of 28 V, using two carrier W-CDMA.

Index Terms — Semiconductor devices, GaN, power amplifiers, intermodulation distortion, code division multiple access, WCDMA, circuit optimization

I. INTRODUCTION

The wireless infrastructure industry today is strongly focused on improving the efficiency of power amplifiers that employ high linearity modulation schemes such as wideband code division multiple access (W-CDMA). Linearity is typically measured in terms of third order intermodulation distortion (IM3), or as preferred for more complex modulation schemes such as W-CDMA, adjacent channel leakage ratio (ACLR). Both are a measure of the amount of distortion generated by an amplifier that will affect adjacent channels in the operation of a multi carrier system.

Conventional linear operation requires back off of the amplifier from saturation to the linear gain region of the amplifier to ensure the intermodulation distortion is kept below system requirements. However with a conventional class A or class AB bias this severely limits the efficiency of the power amplifier. In this mode of operation for WCDMA modulation, a power transistor will typically operate at 8.5 dB back off from the 1dB compressed output power point of the power transistor. This requires the power transistor to typically operate at an power added efficiency 20 % or less at the 2.1 GHz to 2.17 GHz frequency band. For preceding driver and predriver amplifier stages, the devices employed are backed off even further to ensure the distortion requirements of the entire amplifier chain are met.

To improve efficiency, while maintaining linearity performance, a number of circuit and digital signal processing techniques are being employed by wireless infrastructure equipment manufacturers. One such configuration that has increased significantly over the last two years is digital predistortion (DPD) correction. Reasons for the increase in popularity of this technique include:

- 1) Reduced complexity of RF components needed versus other correction techniques such as feed forward amplifiers. This leads to a more compact solution
- 2) Customized correction algorithms can be implemented and adjusted relatively easily using field programmable gate array (FPGA) integrated circuits.

Coinciding with the development of new circuit correction techniques, new semiconductor power device technologies are being developed. Typically digital predistortion configurations have been developed to work with the incumbent power semiconductor technology used in wireless infrastructure today – silicon laterally diffused metal oxide semiconductor (Si LDMOS) transistors. This study focused on linearity and efficiency performance comparison using AlGaN/GaN high electron mobility transistors (HEMT) with a digital pre distortion test system. Previous studies [1]-[2] have focused on continuous wave (CW) analysis of power devices in GaN and SiC. More recent studies have benchmarked AlGaN/GaN based devices against digital predistortion [3]-[4] and against more complex envelope tracking (ET) topologies [5] which further improve efficiency gains.

II. OVERVIEW OF TEST SET UP AND TESTED DEVICES

Figure 1 shows the test set using digital pre-distortion correction. The testing was performed using an established and available digital pre-distortion evaluation board. The DPD board employs digital signal processing to distort the input signal to the power amplifier to correct for the non-linearity of the power amplifier. The resultant output signal of the power amplifier is a reduced distortion modulated signal.

The system uses a modulator, upconverter and driver amplifier to provide the correct transmit frequency and power level to the device under test. Additionally a portion of the DUT output power is coupled into a downconverter and demodulator to provide signal feedback for nonlinearity correction.

A training signal with high peak-to-average power is sent through the system to estimate the required amplitude and phase corrections. The system then enters a continuous adaptation state to further improve the linearity. Any sudden changes in back-off or operating state generally may require repeating the training sequence.

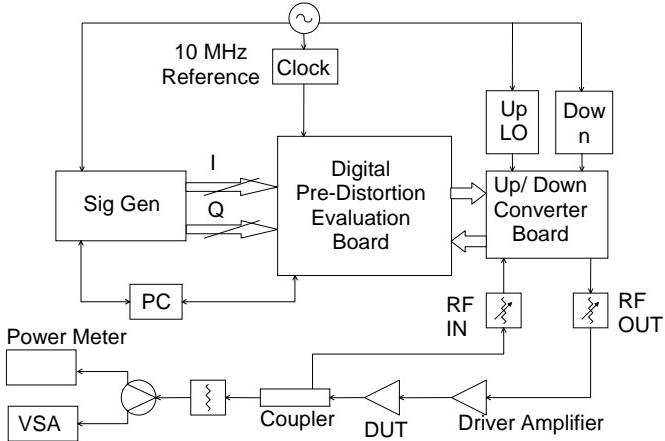


Fig. 1. Block diagram of digital pre-distortion test set up.

AlGaN/GaN HEMTs based on an internally developed process [6] were used as the device under test (DUT) in this system. Typically the devices tested provide a saturated output power density greater than 3 W/mm at a drain voltage of 28 V. These devices are fabricated on a silicon carbide (SiC) substrate for improved thermal dissipation performance at the increased power density over existing semiconductor technologies. Total gate periphery was 20 mm and the process gate length was 0.6 μ m. All devices measured were operated at a drain voltage of 28V with a class AB bias point.

III. COMPARISON OF DEVICE PERFORMANCE TO DIGITAL PREDISTORTION CORRECTED DEVICE

Initial evaluation compared the uncorrected AlGaN/GaN based power amplifier performance to the digital pre-distortion corrected performance of the same device.

Figure 2 shows a single carrier W-CDMA spectral plot at the output of the AlGaN/GaN based amplifier. Test method followed a standard 64 dedicated physical channel (DPCH) test model, peak to average ratio of 10 dB and complimentary cumulative distribution function (CCDF) of 0.01 %.

The arrow points to the adjacent channel power generated by the uncorrected AlGaN/GaN based power amplifier. With digital pre-distortion correction applied the reduced ACLR can clearly be noted.

Figure 3 more clearly describes the performance improvement made using digital pre-distortion correction over the dynamic range of the amplifier at 2.14 GHz. Typically the power amplifier specification for W-CDMA will require ACLR to be below -45 dBc at 5MHz offset. For the uncorrected AlGaN/GaN based power amplifier, this point is marked A on Figure 3. Output power at this limit is 32 dBm with a corresponding power added efficiency (PAE) of 9.5 %. Digital predistortion correction was then applied and the AlGaN/GaN amplifier now operates with the same ACLR limit at the point marked B. Output power can be increased by

7 dB (a factor of 5) to 39 dBm. Additionally PAE improved significantly (by 24 %) to 33 %.

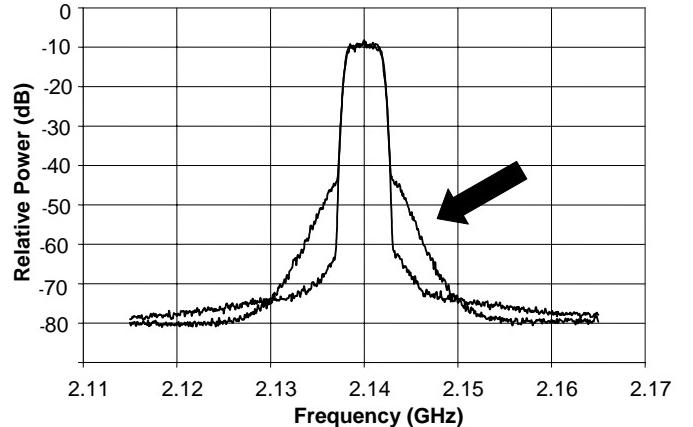


Fig. 2. Spectral plot of single carrier WCDMA 64 DPCH at the output of the AlGaN/GaN based power amplifier. Plot shows the comparison of the GaN power transistor with and without DPD correction applied.

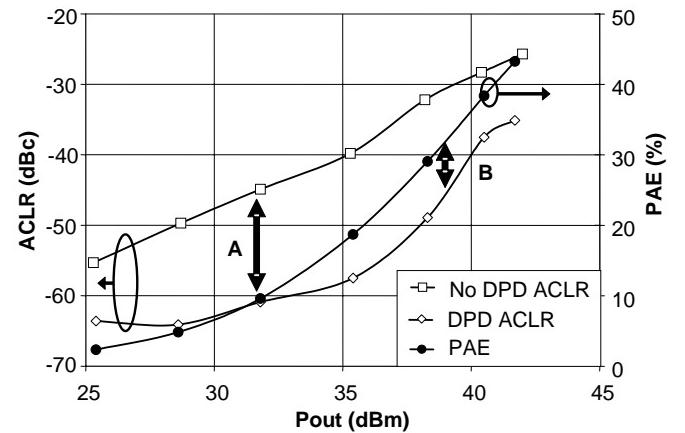


Fig. 3. Comparison of linearity and efficiency performance for a AlGaN/GaN HEMT with and without DPD correction.

IV. BIAS DEPENDENCE OF DIGITAL PREDISTORTION PERFORMANCE

Optimization of the AlGaN/GaN based power amplifier bias was studied. Two separate studies were carried out, first varying the drain current by adjusting the gate voltage device, the second adjusting the drain voltage of the device.

A. Effect of quiescent drain current variation

The AlGaN/GaN HEMTs tested typically have a saturated drain current (I_{dss}) of > 700 mA/mm. The study focused on class AB bias only, varying the quiescent drain current (I_{dq}) from 100mA to 500mA. This range was chosen to understand the trade off between maximized efficiency at the lowest bias point to possible improvement in linearity performance for a

higher quiescent bias point. The drain voltage was fixed at 28 V. Additionally this test was performed using a two carrier W-CDMA signal. Each carrier used standard 64 dedicated physical channel (DPCH) test model. However the DPD correction system does provide some wave shaping to limit the peak to average ratio. Therefore with PAR of 10 dB at the signal generator, the actual PAR at the input of the AlGaN/GaN based amplifier was 8.2 dB.

The results of the varying Idq study are shown in Figure 4. Adjacent channel leakage ratio (ACLR) and power added efficiency (PAE) are plotted versus output power. For lower output power (< 35 dBm) higher Idq shows an improvement of ACLR by up to 5 dB. ACLR levels of -55 dBc to -60 dBc at 5MHz offset are achieved. A higher Idq operation is preferable for predriver and driver amplifier line up stages where such ACLR performance is needed. For output power levels above 37 dBm, lower Idq bias provides the best ACLR performance. Additionally PAE degrades by up to 12 % over the quiescent bias range studied as Idq is increased.

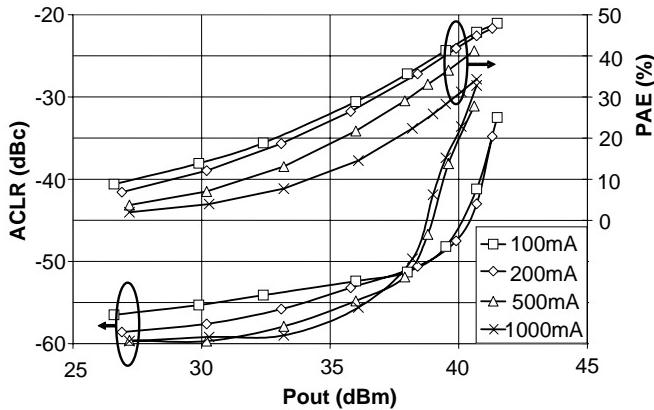


Fig. 4. Effect of AlGaN/GaN transistor Idq variation on linearity and efficiency performance. Test using two carrier WCDMA 64 DPCH signal with DPD correction.

A summary of the output power and efficiency performance at -45 dBc at 5MHz offset ACLR, with varying Idq, is shown in Table I. An excellent compromise bias point of average power versus efficiency is achieved for Idq set to 200mA. This provides a minor drop in efficiency while maximizing average output power at 11W.

It is important to note that the efficiency increases have occurred because the AlGaN/GaN based amplifier is operating at 7 dB to 8 dB back off from the saturated output power of the transistor. Typically existing amplifier solutions for W-CDMA applications will operate at 8 dB to 8.5 dB from the 1 dB compression point (P1dB) of the amplifier which produces significant reduction in power added efficiency at class AB bias. Employing envelope elimination and restoration (EER) or envelope tracking (ET) techniques as used in [5] would further increase the efficiency performance for these AlGaN/GaN based amplifiers.

TABLE I
SUMMARY OF POWER AND EFFICIENCY RESULTS WITH DPD
CORRECTION FOR VARYING DRAIN CURRENT

Vd	Idq	Pout	PAE
28V	100mA	10.5W	44.5%
28V	200mA	11W	43.5%
28V	500mA	7.9W	34%
28V	1000mA	7.7W	23%

B. Effect of drain voltage current variation

The AlGaN/GaN HEMTs tested typically have a gate drain breakdown voltage (BV_{gd}) > 100 V. The study focused on varying the drain voltage (V_d) from 28 V to 48 V. This range was chosen to cover possible practical voltages achievable by infrastructure equipment manufacturers today and to understand possible improvements in linearity performance for a higher drain voltage bias point. The quiescent drain current was adjusted to 500 mA for all measurements. This test was performed using a single carrier W-CDMA signal using 64 dedicated physical channel (DPCH) test model. However the DPD correction system does provide some wave shaping to limit the peak to average ratio. Therefore with PAR of 10 dB at the signal generator, the actual PAR at the input of the AlGaN/GaN based amplifier was 5.6 dB.

The results of the varying drain voltage study are shown in Figure 5. Adjacent channel leakage ratio (ACLR) and power added efficiency (PAE) are plotted versus output power.

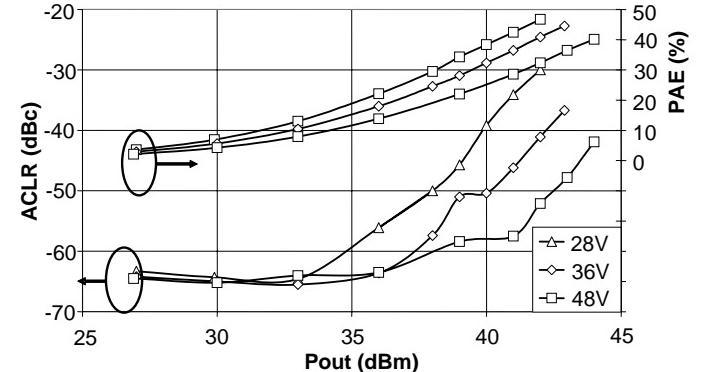


Fig. 5. Effect of GaN transistor drain voltage on linearity and efficiency performance. Test using single carrier WCDMA 64 DPCH signal with DPD correction.

As expected the output power of the AlGaN/GaN based power amplifier increases with increasing drain voltage. As drain voltage increase from 28V to 48V saturated power density of the device increases from 3 W/mm to 5 W/mm (2.2 dB), following linear scaling with voltage.

A summary of the output power and efficiency performance at -45 dBc at 5MHz offset ACLR, with varying V_d , is shown

in Table II. Linear average power increases from 7.9 W, at a drain voltage of 28 V, to 22.9 W, at a drain voltage of 48 V (4.6 dB). Additionally power added efficiency increases from 34 % to 38 % as drain voltage increases from 28 V to 48 V. Both these factors point to improved linear performance of the AlGaN/GaN HEMT for increasing drain voltage operation. This result is expected. As drain voltage increases the amplifier operates further from the knee voltage of the device. Additionally, at 48 V operation the drain voltage is not sufficiently high to be greatly affected by non linearity effects caused by the gate drain breakdown of the device.

Additionally this compares well with results highlighted in [3], which used a 36mm device at higher drain voltage (63V), and [4], which achieved a higher output power but for reduced efficiency due to the larger gate periphery device and push pull configuration used.

TABLE II
SUMMARY OF POWER AND EFFICIENCY RESULTS WITH DPD
CORRECTION FOR VARYING DRAIN VOLTAGE

Vd	Idq	Pout	PAE
28V	500mA	7.9W	34%
36V	500mA	12.6W	36.4%
48V	500mA	22.9W	38%

VI. CONCLUSIONS

AlGaN/GaN HEMTs have been characterized with digital pre-distortion correction. Significant improvements in linearity and efficiency performance using DPD correction have been demonstrated with average power output of 11 W and PAE of 43.5 % for an AlGaN/GaN based amplifier operating at 28 V and a saturated output power of 60 W.

Further study of bias conditions highlights that low quiescent drain current is essential for maximizing efficiency gains. Additionally AlGaN/GaN HEMT linearity and efficiency performance is significantly improved for applications that can operate at 48 V or higher voltages, with average power output of 22 W and PAE of 38 % for an AlGaN/GaN based amplifier operating at 48 V and a saturated output power of 100 W.

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